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User Manual

cPCIBPMC3U64ET

cPCI 3U 4HP 1 Slot PMC Compatible Carrier

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CPCIBPMC3U64ET
cPCI and PMC Compatible Carrier

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Connection of incompatible hardware is likely to cause serious damage.

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Product Description

CPCIBPMC3U64ET is part of the Dynamic Engineering cPCI and PMC Compatible family of modular I/O components. The cPCIBPMC3U64ET adapts one PMC to one cPCI slot.

The cPCIBPMC3U64ET has a “sister” product for 6U applications – the cPCIBPMC6UET. The 3U version has a 64 bit PCI interface definition for the J2 connector and can work in a 32 bit environment. The 6U card has both the 32/64 PCI capability and rear panel IO.

Special features:

- Universal cPCI 3U 4HP.
- Extended temperature range [-40 +85C]
  LED names within quotes:
- LED on PMC Busmode “PMC”
- LED on plus 12V “P12V”
- LED on minus 12V “M12V”
- LED on plus 5V “P5V”
- LED on plus 3.3V “P3.3V”
- LED on 1.8V “P1.8V”
- User selectable secondary VIO.
- 32 or 64 bit operation on either bus
- 66 or 33 MHz operation. With 66 MHz. primary bus speed the secondary bus can be 66 or 33 MHz. Secondary bus can be at a higher rate than the primary bus using optional oscillator option.
- Front panel connector access through cPCI bracket
- Ethernet, Serial and I2C busses available on reserved J2 pins
- JTAG programming support option

The cPCIBPMC3U64ET is ready to use with the default settings. Just install the PMC onto the cPCIBPMC3U64ET and then into the system. There are a few settings to optimize performance.

DIP SWITCH Settings

Please note that the switch numbering and '1' and '0' definitions are per the silk-screen. Closed corresponds to '0' and open to '1' where so indicated in the silk-screen definitions. The '1' and '0' refer to the silk-screen definitions on the DIP-Switches.

Quick reference:
Set the dip switch 1 :"10110000" for 32 bit operation Default (1—8)
Set the dip switch 1 :"10010000" for the x64 operation (1—8)
Set the dip switch 2 :"01011000" for the x32,64 Default (1—8)

SW1 DIP SWITCH Settings

Select the "green power" clock setting. With the new revision of the bridge [PLX 6466] the secondary clock can be set to be driven low or continue to operate when in the power down state. With the **DIP switch 1** set to '1' the clock will be driven low during power down, and with the switch '0' the clock will always be driven. The factory setting is '0'. **BPCC_EN** is the signal controlled with switch 1.

Select the Bridge "S_CLKOFF". The bridge can drive or not drive the CLK outputs. With a standard PMC installed the clocks should be enabled. With **switch #2** set to '0' the clocks are enabled, with the switch in position '1' the clocks are disabled. **CLK_OFF** is the signal controlled with switch number 2. The factory setting is '0'.

Select the Bridge "DEV64#". The bridge can accommodate 32 and 64 bit cards installed into the PMC slot. With **switch #3** set to '1' the bridge will read the installed PMC to be 32 bit. With the switch set to '0' the bridge will report a 64 bit device. The factory setting is '1'. Please note that the hardware will detect the ACK64# signal to determine the port width for transactions.

PBOOT is selected with **Switch #4**. When '0' the secondary port is selected for "Boot Priority". When '1' the primary port is selected. The PBOOT setting has meaning when in the non-transparent modes. The factory setting is '1'.

MSK_IN is selected with **Switch #5**. When '0' the Bridge clock outputs are enabled. When '1'' the bridge clock outputs are disabled. Both Mask and ClockOff need to be disabled for normal operation. The factory setting is '0'.

UMODE is selected with **Switch #6**. When '1' and in non-transparent mode the bridge will be configured to be a "universal bridge". The factory setting is '0'.

TRANS# is selected with **Switch #7**. When '0' the bridge will act in transparent mode. When '1' the bridge will be in non-transparent mode. The factory setting is '0'.

Select the secondary side [PMC] PCI bus frequency. The options are to use the PCI bus speed [primary] or to force 33 MHz on the secondary side. The PMC to be installed must be 66 MHz compliant to use the 66 MHz secondary side option. The speed is controlled with the **DIP switch #8** position. '1' = 66 MHz capable secondary side. '0' = 33 MHz. **SM66EN** is the signal name controlled by the switch. The factory setting is '1'.

The SM66EN signal is also routed to the PMC connector pin M66EN. If the PMC uses the M66EN as an input then the dipswitch can be used to control the frequency. If the PMC uses the M66EN pin as a control, then the Switch may have no effect. For example if the switch is in the '1' position and the PMC is selecting M66EN = '0' then the PMC will "win" and the signal will be at the 33 MHz setting. Both the dipswitch and the PMC M66EN have to be enabled for 66 MHz. .

SW2 DIP SWITCH Settings

DIPSWITCH #2 [SW2 table on silk-screen]

Switch #1 selects the secondary side VIO [**SVIO**]. When the switch = '1' 3.3V is selected for the secondary side. When '0' is selected 5V is the VIO definition. The VIO plane is a reference for the IO level. The specification does not prohibit larger current consumption from these pins. The cPCIBPMC6UET design utilizes a MOSFET to control the 5V or 3.3V rails onto the VIO plane. Max consumption on the VIO rail is 3A. The factory setting is '0'.

Switch #2 selects the clock reference to use for the secondary side. "1' selects the PCI clock from the primary side and '0' selects the installed oscillator. The oscillator has a default frequency of 66 MHz. Please note that the secondary side frequency still depends on the M66EN definition – the bridge will divide the clock if set to 33 capable. The factory setting is '1'.

Switch #3 selects the addressing mode. When '1'the Private memory space is selected for the secondary side, when '0' the standard memory map is selected. The factory setting is '0'. **PRVDEV/XBMEM** is the signal controlled by this switch. It is recommended to read the PLX manual on the 64/66 when this signal is to be used.

Switch #4 selects **Primary PLL** enabled or not. '1' disables the PLL and '0' enables the PLL. The factory setting is '1'. In most cases the primary PLL will be disabled.

Switch #5 selects **Secondary PLL** enabled or not. '1' disables the PLL and '0' enables the PLL. The factory setting is '1'. In most cases the secondary PLL will be disabled. If selecting an external clocking option for the PMC or using the OSC option please consult the PLX manual for specific switch options.

Switch #6 selects **PMC IDSEL** range. '0' selects the lower range using AD16 . '1' selects the upper range using AD20 The factory setting is '0'.

Switch #7 selects **PMC Monarch Mode**. For PrPMC's using the Monarch Mode pin, closing the switch ['0'] will cause the Monarch Pin [64] at the PMC to be tied through a 1KΩ resistor to ground. With the switch open the Monarch pin is tied to 3.3V through 4.7KΩ. The factory setting is '0'.

Switch #8 is spare

Interrupts

Interrupts from the PMC's are connected from the PMC to the primary PCI bus. INTA through INTD are mapped directly to the primary bus segment.

Options

Dynamic Engineering offers options to the cPCIBPMC6UET design.

The J2 connector when configured for the upper PCI bus has some unallocated pins which have alternate uses. The I2C, Serial ports and Ethernet pins associated with the PMC can be routed to these pins. The connections are isolated with series resistors to allow them to be installed or not. The default is not. Please contact Dynamic Engineering if you would like to have these signal connected. The connections are shown in figure 1.

Other Signals

PME is tied between the cPCI connector and the PMC positions bypassing the bridge as a standard setting. The bridge can be inserted into the path if desired. Resistor jumpers are used for this option. Please contact Dynamic Engineering for this option.

Reset Out on PMC position 0 is tied to Reset In on the secondary side of the bridge. The signal is pulled-up for non-PrPMC implementations. This connection will allow the PrPMC to cause a reset to the local side of the bridge. More details are available in the PLX 6466 data book.

JTAG support is available. The JTAG header position is clearly marked in the silk screen. The header is frequently not used and is not installed unless requested. Please contact Dynamic Engineering for this option.

The Bridge supports a GPIO function. A header position is available with the positions clearly marked in the silk-screen. The header is installed by request. Please contact Dynamic Engineering for this option. The lower 4 bits are terminated with 4.7KΩ to 3.3V. The upper bits have internal [bridge] pull-ups.

Options

Dynamic Engineering offers three versions of the cPCIxPMC design.

cPCI2PMC is a passive implementation. The cPCI connections on the cPCI2PMC are longer, and can limit the number of cards or adapters on a particular bus segment. The passive design has “0” delay between the primary PCI bus and the PMC. The VIO and bus speed definitions are common to the primary PCI bus and PMC.

CPCIBPMC(ET) is bridged, isolating the PMC from the cPCI bus. cPCI connections are specification compliant on the cPCIBPMC. cPCIBPMC can be used in multiple slots on the same PCI bus segment. The bridged design has pipeline delays between the primary and PMC buses. The bridged design has independent VIO definitions between the PMC and the primary bus.

In addition to the basic bridged or not bridged versions there are options for Ethernet, Serial ports, and I2C.

Some PMCs support Ethernet connections over the Pn4 connector with pins specified by the PICMG standard 2.15. cPCIBPMC supports Ethernet capable cards with an optional connections to the J2 connector.

Some PMCs support serial channels on Pn4 with pins specified by by PICMG standard 2.15. cPCIBPMC supports serial capable cards with optional connections to J2.

In addition the cPCIBPMC has options for I2C signal routing. The signals are routed from Jn1 to J2.

All optional signals can be isolated or added with resistor packs located to create short stubs when the signals are not in use.

PMC Module Backplane IO Interface Pin Assignment

The figure below gives the pin assignments for the PMC Module IO Interface – from Pn4 to the cPCIBPMC3U64-J2 connectors. Also see the User Manual for your PMC board for more information.

CPCI J2			Pn4	
A19	A21	E0TRDOP/E0TRD2P	1	2
B19	B21	E0TRD0N/E0TRD2N	3	4
			5	6
D19	D21	E0TRD1P/E0TRD3P	7	8
E19	E21	E0TRD1N/E0TRD3N	9	10
			11	12
A16	A18	E1TRD0P/E1TRD2P	13	14
B16	B18	E1TRD0N/E1TRD2N	15	16
			17	18
D15	D17	E1TRD1P/E1TRD3P	19	20
E15	E17	E1TRD1N/E1TRD3N	21	22
			23	24
			25	26
	C1	TXD0	27	28
	B2	TXD1	29	30
			31	32
	C3	RXD0	33	34
	B4	RXD1	35	36
			37	38
			39	40
			41	42
			43	44
			45	46
			47	48
			49	50
			51	52
D1		TXD2	53	54
D3		TXD3	55	56
			57	58
E1		RXD2	59	60
E3		RXD3	61	62
			63	64

FIGURE 1 CPCIBPMC3U64 PN4 INTERFACE STANDARD

The I2C connections are
from Pn1-41 = I2C-CLK to J2-A3
Pn1-42 = I2C-DTA to J2-A2

Applications Guide

Interfacing

Some general interfacing guidelines are presented below. Do not hesitate to contact the factory if you need more assistance.

Installation
The PMC is mounted to the cPCIBPMC-ET prior to installation within the chassis. For best results: with the cPCI bracket installed, install the PMC at an angle so that the PMC front panel bezel penetrates the cPCI bracket then rotate down to mate with the PMC [PnX] connectors.

There are four mounting locations. Two into the PMC mounting bezel, and two for the standoffs near the PMC bus connectors.

Start-up
A third party PCI device cataloging tool will be helpful to check that the VendorID and CardID are “seen” by the OS.

Watch the system grounds. All electrically connected equipment should have a fail-safe common ground that is large enough to handle all current loads without affecting noise immunity. Power supplies and power consuming loads should all have their own ground wires back to a common point.

Power all system power supplies from one switch. Connecting external voltage to the PCIBPMC-ET when it is not powered can damage it, as well as the rest of the host system. This problem may be avoided by turning all power supplies on and off at the same time. This applies more to the PMC installed into the cPCIBPMC-ET than the cPCIBPMC-ET itself, and it is smart system design when it can be achieved.

Construction and Reliability

The cPCIBPMC is constructed out of 0.062 high temp ROHS compliant material. Gold has been used for plating rather than Tin for improved performance over time.

Surface mounted components are used. The connectors are SMT for the PMC bus and through hole [compression fit] for the cPCI. The PMC Module connectors are keyed and shrouded with Gold plated pins on both plugs and receptacles. They are rated at 1 Amp per pin, 100 insertion cycles minimum. These connectors make consistent, correct insertion easy and reliable.

The PMC Module is secured against the carrier with the PMC connectors. It is recommended, for enhanced security against vibration, that the PMC mounting screws are installed. The screws are supplied with the PMC from the OEM. Dynamic Engineering has screws, standoffs, blank bezels and other PMC hardware available at a reasonable cost if your PMC was not shipped with some of the required attachment hardware or if it has been misplaced.

Thermal Considerations

If the PMC installed has a large heat dissipation; forced air cooling is recommended.

Warranty and Repair

Please refer to the warranty page on our website for the current warranty offered and options.

http://www.dyneng.com/warranty.html

Service Policy

Before returning a product for repair, verify as well as possible that the suspected unit is at fault. Then call the Customer Service Department for a RETURN MATERIAL AUTHORIZATION (RMA) number. Carefully package the unit, in the original shipping carton if this is available, and ship prepaid and insured with the RMA number clearly written on the outside of the package. Include a return address and the telephone number of a technical contact. For out-of-warranty repairs, a purchase order for repair charges must accompany the return. Dynamic Engineering will not be responsible for damages due to improper packaging of returned items. For service on Dynamic Engineering Products not purchased directly from Dynamic Engineering contact your reseller. Products returned to Dynamic Engineering for repair by other than the original customer will be treated as out-of-warranty.

Out of Warranty Repairs

Out of warranty repairs will be billed on a material and labor basis. The current minimum repair charge is $100. Customer approval will be obtained before repairing any item if the repair charges will exceed one half of the quantity one list price for that unit. Return transportation and insurance will be billed as part of the repair and is in addition to the minimum charge.

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Specifications

Logic Interfaces:	PCI Interface 33/32 <–> 66/64
Access types:	PCI bus accesses
CLK rates supported:	33 or 66 MHz PCI clock rates
Software Interface:	transparent Bridge. PLX6466 registers in configuration space
Initialization:	Selections for VIO, primary and secondary clock rates
Interface:	PMC front bezel via cPCI bracket. Additional optional Ethernet, Serial and I2C connections via J2.
Dimensions:	3U 4HP
Construction:	High Temp ROHS compliant Multi-Layer Printed Circuit board, Through Hole and Surface Mount Components. ROHS processing available by adding –ROHS to part number.

Order Information

standard temperature range –40 - +85ºC

cPCIBPMC3U64	3U 4HP cPCI card with PMC position http://www.dyneng.com/cpcibpmc3u64.html
cPCIBPMC3U64-ENET	3U 4HP cPCI card with PMC position and RP Ethernet, Serial and I2C connections http://www.dyneng.com/cpcibpmc3u64.html

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